Integrated Systems Laboratory- www.iis.ee.ethz.ch

Curriculum Vitae

Prof. Andreas Schenk

Professor for Nano-Device Physics
schenk@iis.ee.ethz.ch

Degrees/Higher Education

1987	PhD, Theoretical Physics, Humboldt University of Berlin (HUB) Germany
1981	Dipl. Phys., Theoretical Physics, Humboldt University of Berlin (HUB) Germany

Professional Career

2004 - present	Professor for Nano-Device Physics at the Integrated Systems Laboratory of ETH Zurich
1997 – 2004	Scientific Adjoint (Privat-Dozent) at the Integrated Systems Laboratory, D-ITET, ETH Zurich
1991 – 1997	Postdoc at Integrated Systems Laboratory, D-ITET, ETH Zurich
1988 – 1991	R&D member of WF Berlin GmbH and Research Assistant at Department of Semiconductor Theory of HUB
1987 – 1988	Research Assistant at Department of Semiconductor Theory of HUB

Professional Activities

- Editor - IEEE Transactions on Electron Devices
- Work package leader FET Pilot Flagship project Guardian Angels
- Work package leader ICT STREP project ATEMOX
- Technical Program Committee ESSDERC, IWCE, SISPAD
- Reviewer for JAP, IEEE-TED, Solid-State Electronics, and other journals
- Reviewer of external dissertations, habilitations, and projects proposals

Major Honors and Awards

1997 Granting of Professor of ETH Zurich (Titularprofessor)

Membership in Societies

- German Physical Society (DPG)
- Association of Swiss University Professors

Publications

- 74 peer-reviewed journal publications
- 82 conference publications (proceedings)
- 20 invited talks
- 1 book authored, 2 books co-authored

Achievements

- Theory of non-radiative multiphonon recombination in strong electric fields
- Generalization of Shockley-Read-Hall theory (coupled defect-level recombination)
- Physics-based TCAD models for phonon-assisted band-to-band tunneling, defect-assisted tunneling, direct gate tunneling, Schottky contacts, hot-carrier mobility, band gap narrowing, incomplete ionization, high-temperature effects on generation rates, and long-term charge loss in EPROMs
- Theory for BEEM experiments
- Theory for large ideality factors in solar cell diodes
- Simulation package for single-electron transistors, quantum point contacts, and ballistic MOSFETs
- Device simulation modules for quantum confinement, high-frequency noise, and low-frequency noise
- In-house simulation package for semiconductor micro- and nanodevices (incl. NEGF, MISO, CBOPMC, energy-balance, noise, density gradient)

Teaching

- Semiconductor Devices: Physical Bases and Simulation
- Semiconductor Transport Theory and Monte Carlo Device Simulation (together with F. Bufler)
- Integrated Systems Seminar

Keywords

- Device physics and numerical device simulation
- Quantum transport in nanodevices
- TCAD models
- Simulation of solar cells

Future priority areas

- Ultra low-power and post-CMOS devices
- Advanced numerical methods in device simulation
- Quantum transport
- 3rd generation photovoltaics
- Modelling of energy harvesting systems

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Prof. Andreas Schenk - Research Highlights

Nano-Device Physics

Focus

The Nano-Device Physics Group focuses on modeling of micro- and nanoelectronic devices by numerical simulations based on semiconductor physics (Technology Computer Aided Design - TCAD). The TCAD research activities concern first-principle modeling of carrier transport, simulation of quantum structures, ab initio and molecular dynamics simulation for diffusion and activation. Scientific challenges are future generation manufacturing technologies, devices in the nanometer regime, quantum transport, ultra shallow junction leakage, post-CMOS und emerging research devices. These research activities are closely coupled with physical characterization and electronic measurement groups of our laboratory to validate the results of TCAD.

New transistor generations

As stated by the International Technology Roadmap for Semiconductors, field effect transistors (FETs) with sub-10-nm channel length will be manufactured in 2016 for the HP22 technology node while 5 nm channel lengths will be required for the HP14 node in year 2020. Nanoelectronic research is partially concerned with the development of novel multi-gate device architectures to improve the electrostatic integrity. Nanowires are attractive not only from an electrostatic point of view, but also due to their capability to act both as FETs and connectors. Technology computer aided design (TCAD) can be used to support the fabrication of such novel devices by means of preliminary simulations to investigate their features and performance limits. The use of quantum mechanics is mandatory here, since typical dimensions are of the order of the de Broglie wave length. Fig. 1 shows nanowire transistors with different cross sections subject to atomistic simulations.

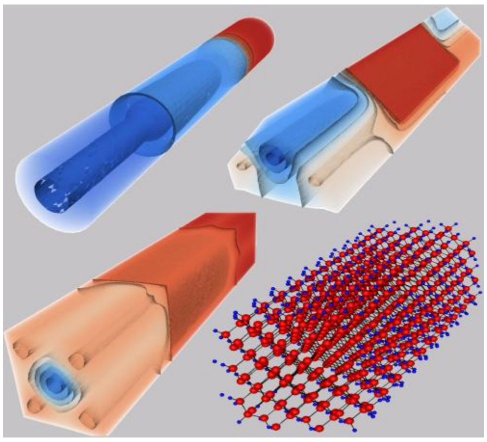

Figure 1: Quantum transport modeling of silicon nanowire transistors: equipotential surfaces for different cross sections and atomic lattice

Quantum transport simulation including band structure effects and dissipative scattering

Due to its simplicity, the effective mass approximation (EMA) is a widely used approach within nowadays quantum transport simulators. However, the EMA becomes violated for nanowires with small (typically ≤ 5 nm) diameters. In this regime atomistic approaches ranging from empirical tight-binding methods to fully ab-initio approaches are preferred. Fig. 2a shows the probability density in a silicon nanowire computed by the empirical pseudo-potential method.

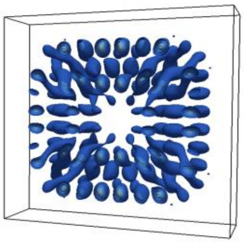

Figure 2a
Highest occupied molecular orbital of a silicon nanowire with surfaces oriented along the <110> direction. Shown are iso-surfaces of the square of the wave function.

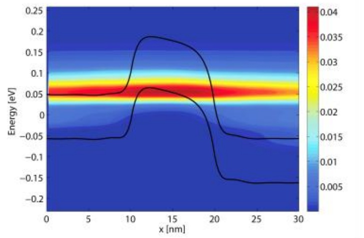

Figure 2b
Spectral current of a silicon triple-gate nanowire FET with 10 nm gate length at V_{GS} = 0.2 V and V_{DS} = 0.1 V. The two lowest subbands are also displayed.

If the phase information of the wave function is preserved throughout the device, a ballistic transport description can be applied which eventually provides the theoretical limit for the device performance. The ballistic limit also allows to go beyond the EMA. In the non-equilibrium Green's Function formalism as the ultimate framework to simulate quantum transport, phonon scattering can be incorporated in the so-called self-energies by a perturbative approach. However, the interdependence between self-energy and Green's functions leads to a massive increase of the computational burden. An interesting consequence of inelastic phonon scattering is that only the total current is conserved, while the spectral current may change. Fig. 2b shows the current crowding on top of the source-drain barrier in the subthreshold regime of nanowire FETs due to inelastic phonon scattering in the source extension next to the barrier.

Ultra low-power devices for energy-autonomous systems

The goal of dramatically-reduced power consumption in digital CMOS circuits can only be addressed by removing the limitation given by the non-scalable subthreshold slope (SS). In conventional CMOS transistors the SS is limited to the room-temperature limit of 60 mV/dec because of the Boltzmann tail of Fermi-Dirac statistics. Novel device concepts for the beyond-CMOS era comprise tunnel FETs (T-FETs), negative capacitance (NC) FETs, superlattice based (SL) FETs, spin- FETs, carbon nanotube (CNT) FETs, and graphene-based FETs (G-FETs). T-FETs potentially enable energy efficient circuits with power supply lower than 0.5 V. So far produced T-FETs have in common that the steep slope voltage interval is narrow at an extremely low current level and that the on-current falls short of that of conventional FETs. However, both Ge and InAs based T-FETs show advantages in energy-delay-product and switching delay as the supply voltage is scaled towards 0.25 V. Current research tries to improve the on-current by using Si/III-V hetero junctions, which provide weaker tunnel barriers and the possibility to tune the band line-up from staggered to broken.

By combining ultra low-power electronics with new sources of energy production, the FET Pilot Flagship project Guardian Angels is searching for systems that will be powered with energy taken from their immediate environment. More information on http://www.ga-project.eu.

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